Quantum Architecture: From Devices to Systems

Workshop on Quantum Information Science – Vienna, VA
April 24, 2009

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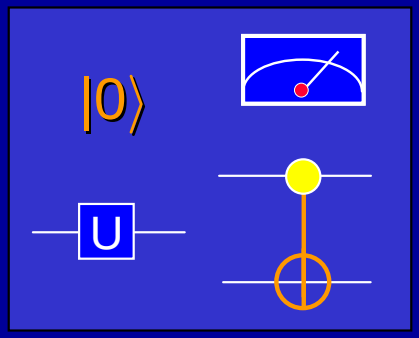
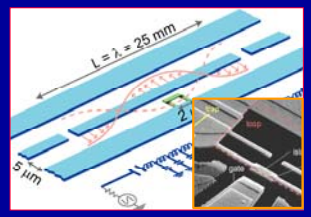
The Q. Architecture Challenge

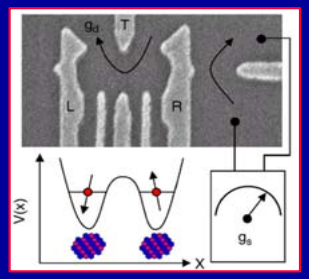


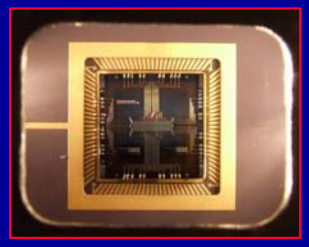
DiVIncenzo

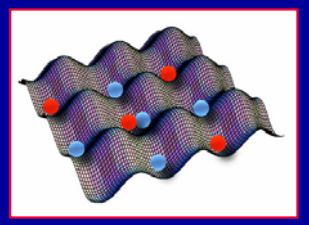
1. Qubits
2. Universal gates
3. Input state
4. Measurement

Theory

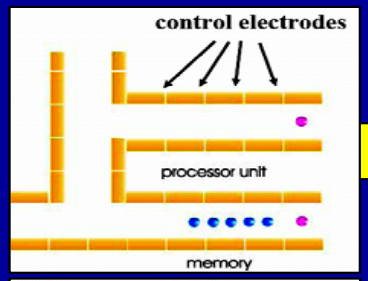


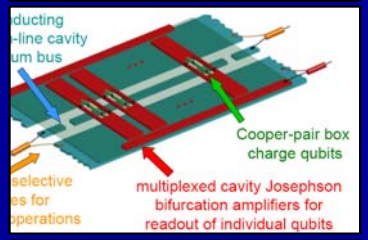


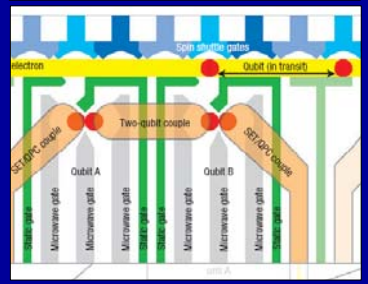


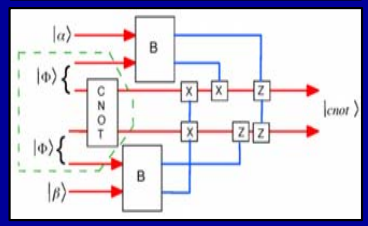


Devices









Technology

Architectural Design

?

Systems

Lessons learned… ?

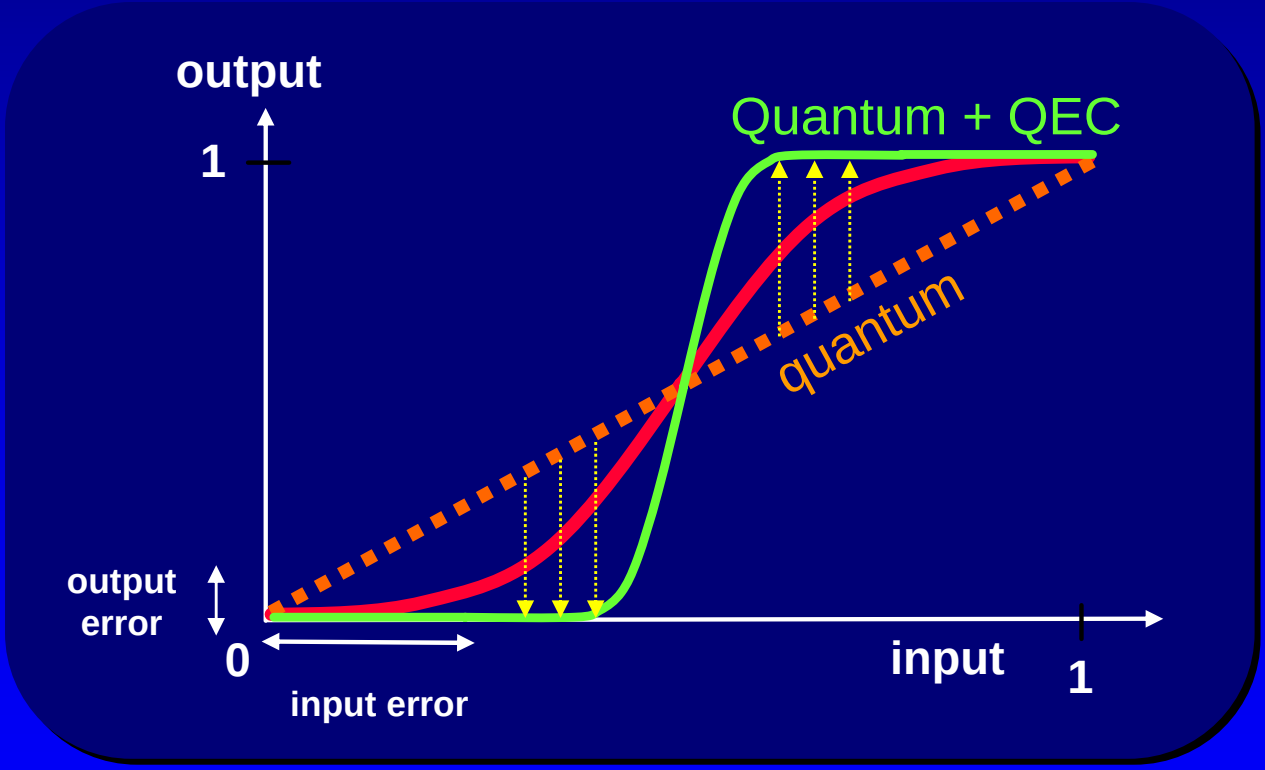
Architecture: Lessons

Devices + Architecture = System which is…

1. **Reliable**
2. **Parallelizable**
3. **Programmable**
4. **Debuggable**
5. **Predictable**

Device Scalability

- Why are vacuum tubes (or CMOS) scalable?



- Quantum gates are intrinsically unstable!
- Need a different approach: Error Correction

Fault Tolerance Theorem

Reliable computers can be constructed from faulty components

- A circuit containing N (error-free) gates can be simulated with probability of error at most ε, using $N \log(N/\varepsilon)$ faulty gates, which fail with probability p, so long as $p < p_{th}$. von Neumann++ (1956)

Quantum version: Shor, Preskill, Aharonov, Ben-Or, Knill, Laflamme, Zurek, …

Fault Tolerance & QC

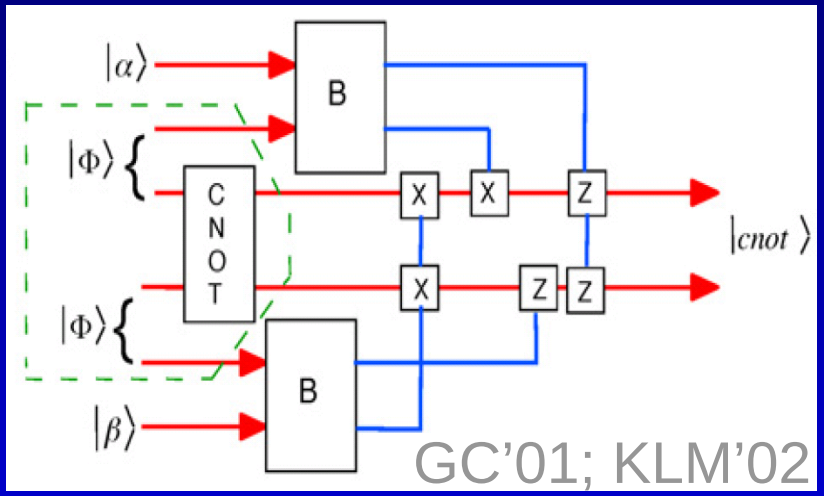
- In a FT QC, >99% of resources spent will probably go to quantum error correction!

The requirements for fault-tolerance determine how a quantum computer may be physically realized

- Max device err p_{th} = (# ways to get > 1 error)$^{-1}$

Case Study: Linear Optics

- **Capability:**
  - **Reliable single qubit ops**
  - **CNOT with $p_{fail} \sim$ 89%**



GC'01; KLM'02

- **Recipe:**
  - **Repeat ancilla states creation until successful**
  - **Rely on good photon-number measurements**

Ralph, Rep. Prog. Phys. **69** (2006)

- p_{th} **< 3× 10^{-3} photon loss, 10^{-4} depolarization**
- **Need ~10^{20} bell pairs per operation!**

Dawson, Haselgrove, Nielsen, PRL **96,** 020501 (2006) ; quantph 0601066

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Q Factoring: Space vs Time

- Problem: Factor N bit number
- Shor's algorithm needs

$\sim N$	$\sim 2N^2$	$\sim N^3$	qubits
$\sim N^3$	$\sim 9N(\log^2 N)$	$\sim \log^3 N$	steps

- Ex: N=663 ➡ 10^6 qubits, $\sim 10^6$ ops
  150 hours (1Hz QC) ...6 days!

Fowler, Devitt, Hollenberg, QIC 4 p237, 2004

Scheduling Q. Resources

- Problem: qubit movement & gates
- Results:
  - QUALE (U. Wash.): map q. circuit onto physical layout, using Path-Finder (ions)
  - QPOS (U. Davis): schedule physcal ops; classical instr. scheduling heuristics (dots)
  - QPU toolchain (Princeton): stagger ops to optimize fault tolerance (e^- on LHe)
  - Quantum CAD (Berkeley): dataflow-analysis; greedy congestion relief (ions)

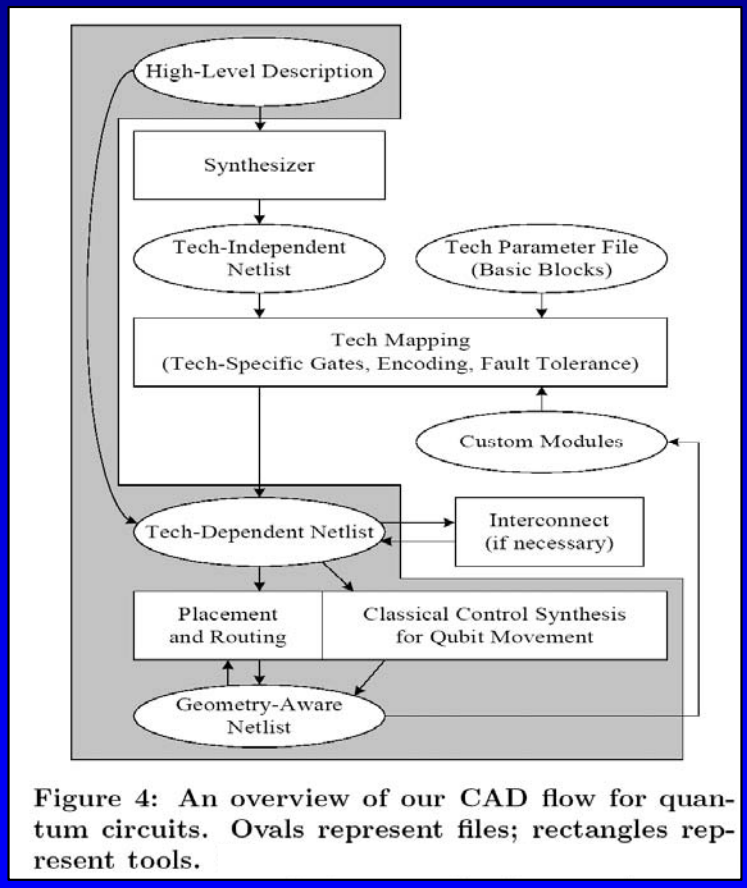

Figure 4: An overview of our CAD flow for quantum circuits. Ovals represent files; rectangles represent tools.

Chi, Lyon, Martoniso ISCA 2007 ; Whitney, Isailovic, Patel, Kubiatowicz CCOF 2007;
Metodi et al Proc. SPIE 2006 ; Balensiefer, Kregor-Stickles, Oskin ISCA 2005

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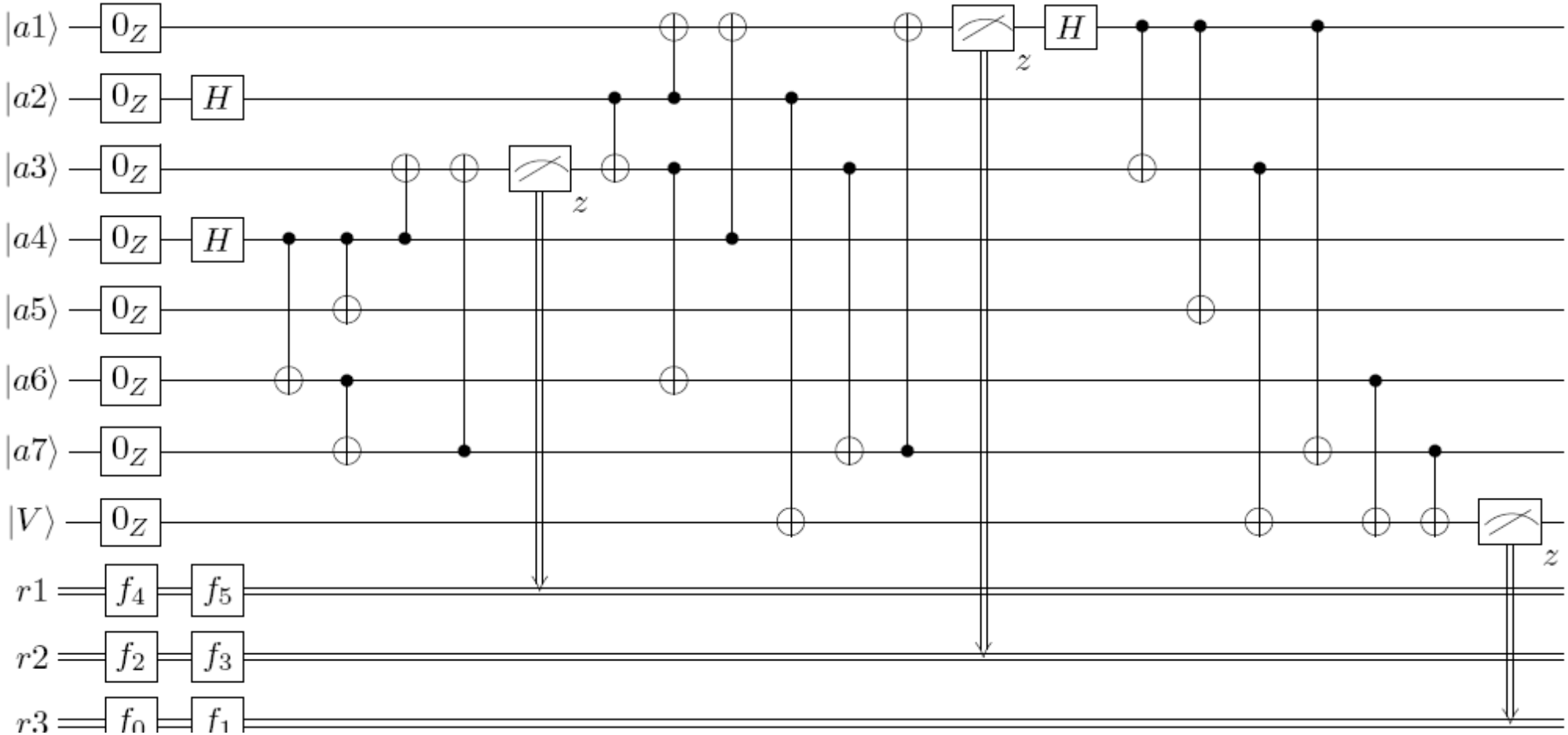
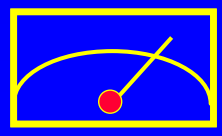
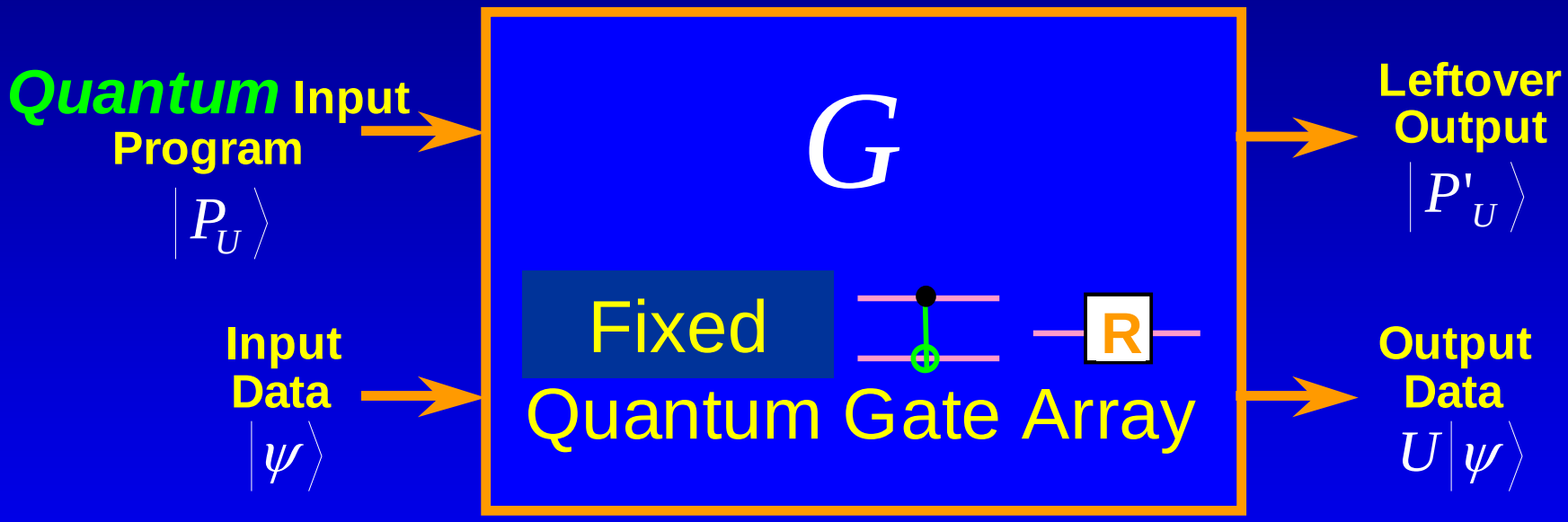
Quantum Circuit Model



- CNOT + single qubit gates, $|0\rangle$, 

Quantum controlled QC



Model: teleport gates...

Catch – only certain programs efficiently implementable

Quantum Software

- Universal, Fault Tolerant QC:
  - Single qubit operations
  - Bell basis measurements
  - A supply of entangled states

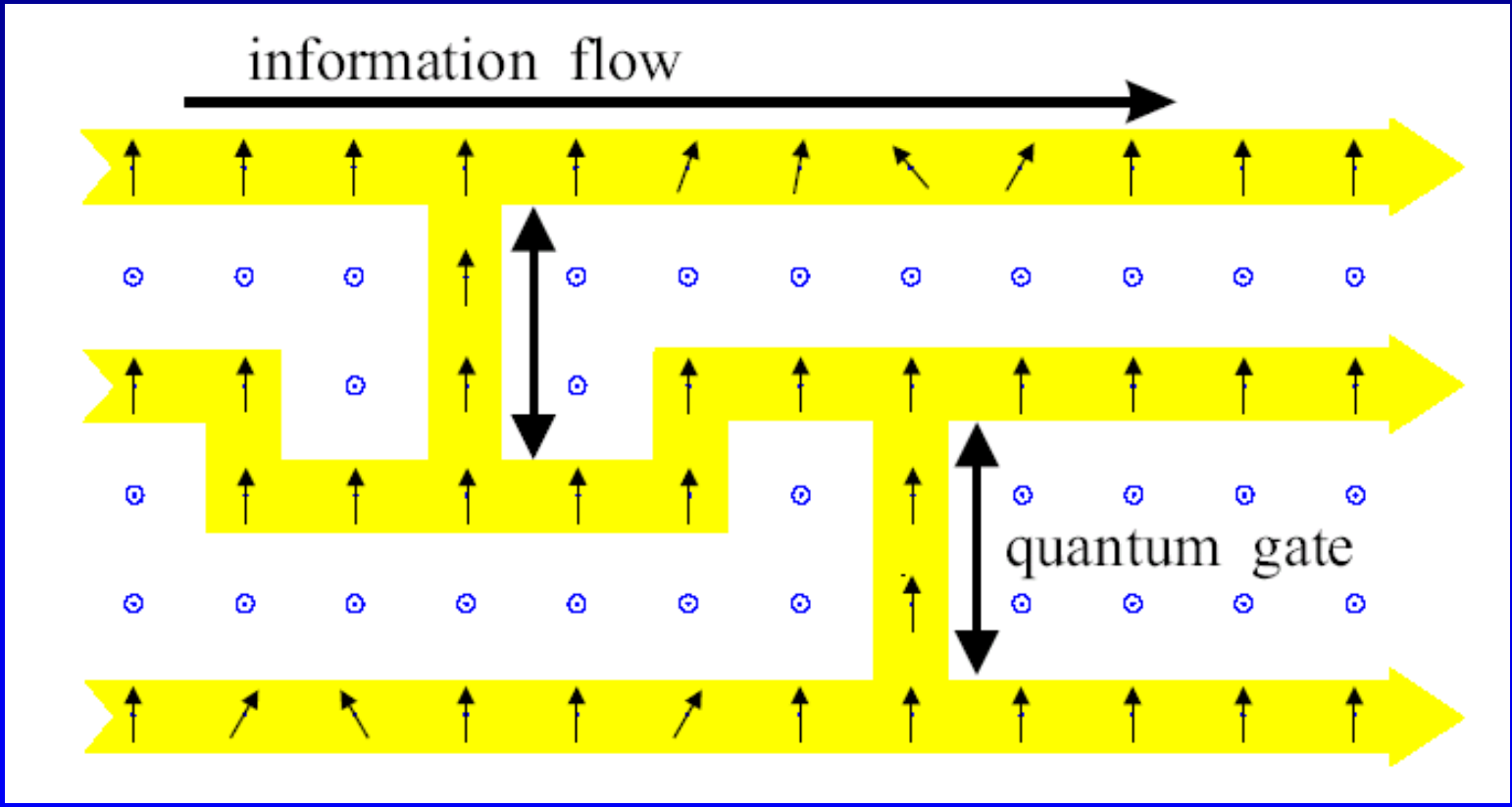
D. Gottesman, I. Chuang, Nature, v402, p390, 1999

Quantum: uncopyable & single-use!

- Inherently hold value - marketable commodities
- Significantly simplify hardware requirements
  - Can be checked at the factory
  - Delivered via a “quantum internet”

Measurement-based QC

R. Raussendorf and H. J. Briegel. PRL 86(22):5188–5191, 2001



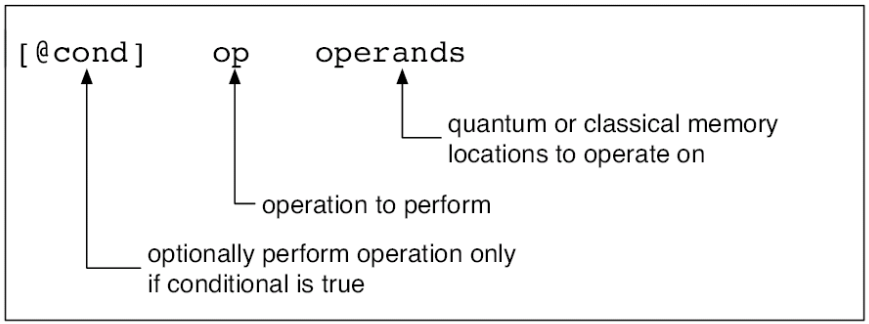
- **Recipe: Create state, then measure**

"measurement" based models of QC

Q. Programming Languages

- **Highly active field!**
  - **QRAM (Knill'96): register machine**
  - **QCL (Omer'98-'03): C-like**
  - **Quantum λ-calculus (Maymin'96,…)**
  - **QML (Altenkrich & Grattage'05): q. control & data**
  - **Meas. QC (Danos et al'04,…): patterns**
  - **QPAlg (Jorrand'04-…): formal verification**
  - **Q-HSK, SQRAM, Q-gol, qGCL…**
- 100 papers (1996-2007)
- Open issue: fault tolerance?

Instruction set format:



Quantum Operations:

h	qN	Basic quantum primitives such as Hadamard (H), invert (X), invert phase (Z), arbitrary rotation (R), and phase gate (S)
x	qN	
z	qN	
rot	qN,real	
s	qN	
v	qN,qC,real	rotate qN about X axis, conditional on qC, by real
cnot	qN,qC	flip qN conditional on qC
swap	qN1,qN2	swap qN1 and qN2
toffoli	qN,qC1,qC2	flip qN conditional on qC1, qC2
measure	cT, qN	measure qN place result in cT

QUALE (U. Washington)

S. Gay, "Quantum Programming Languages," Math. Struct. In Comp. Science 2006

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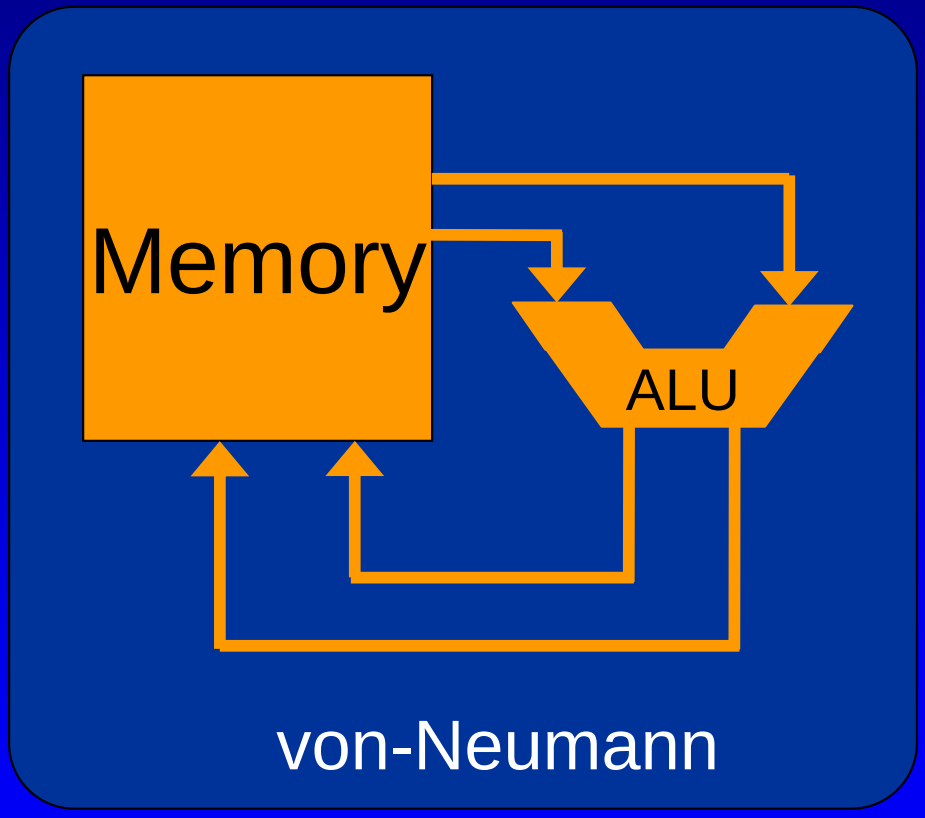
Architecture Concepts

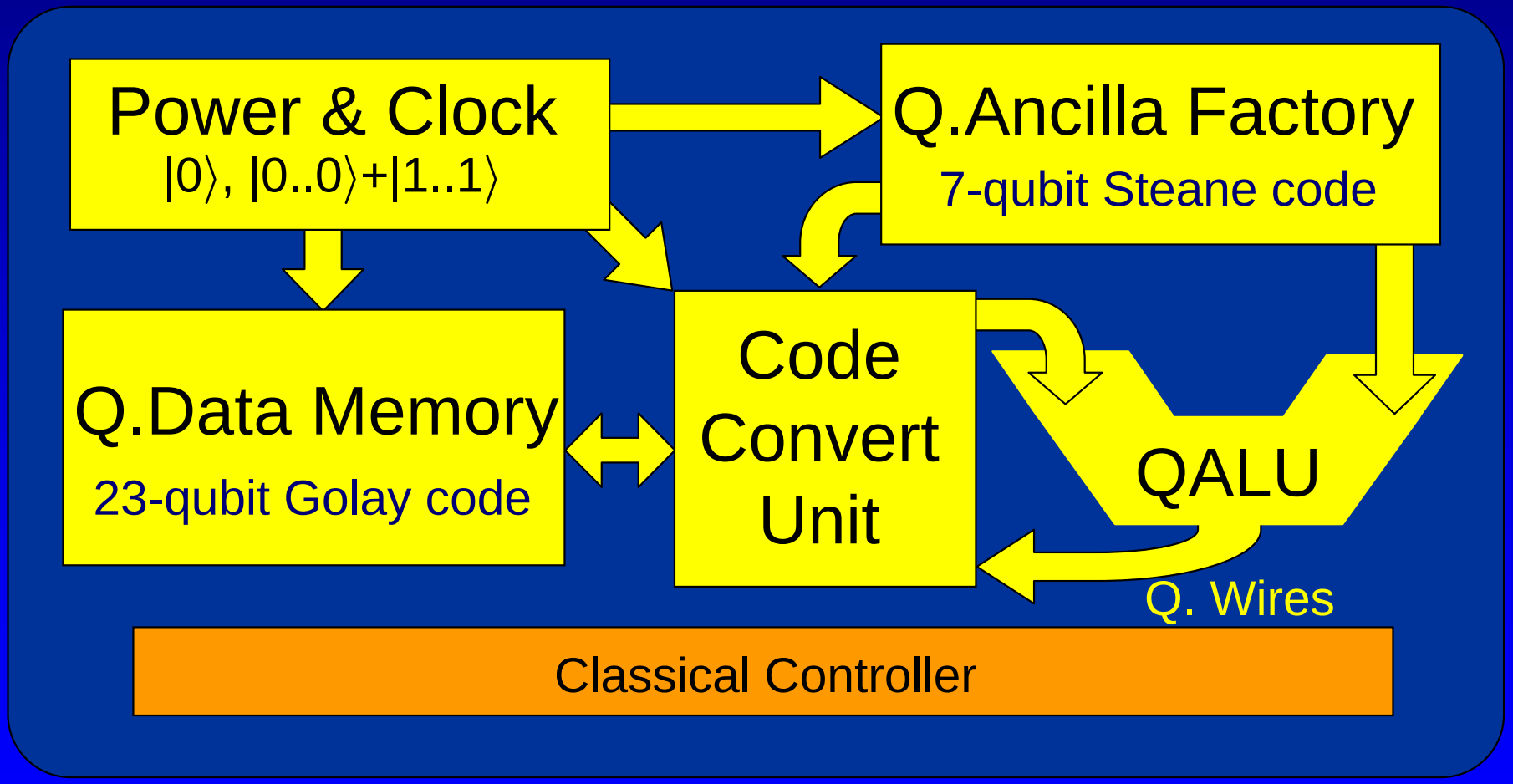
- 1940's: von Neumann – Programmable Systems



- Stored program ; modular design
- Blocks simplify debugging!

Architecture Concepts

- **Modern Q. computer arch. = seek reliability**



Knill; Nielsen & Chuang; Steane ;
Chong, Chuang, Kubiatowicz, Oskin – IEEE Computer 2006

Architecture: Lessons

Devices + Architecture = System which is…

1. **Reliable** > 99% of QC = Error Correction
2. **Parallelizable** Depth / Time / Movement Tradeoff
3. **Programmable** Many new models ; FT lang?
4. **Debuggable** Wires = teleport ; power = entanglement
5. **Predictable**

Real large-scale computing systems are designed & verified far in advance of implementation, with predictive tools

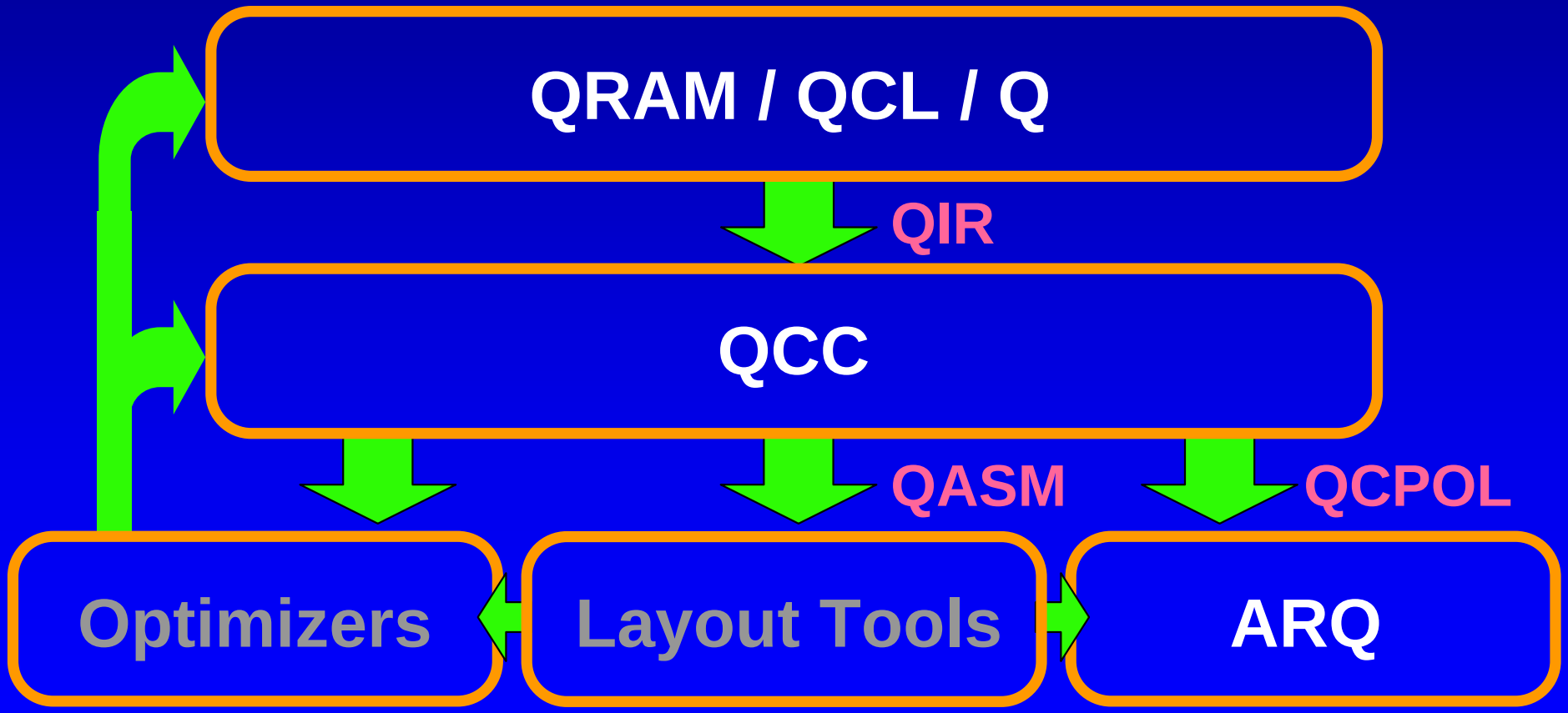
Whirlwind → SPICE → …
Behavioral synthesis → Formal verification → Physical verification

Large Scale, Reliable QC

- System: 10^6 qubits, >10^6 logical gates
- FTQC ~10^7 to 10^8 qubits & physical gates
  (7-qubit Steane code, 1-2 concat. levels)
- Questions:
  - How many lasers required? Laser power?
  - How large an ion trap chip?
  - What kind & size of classical control?
  - What fault tolerance threshold?
    (gate / state / memory / movement)
- Approach: Simulate QECC (efficient!)

Quantum Design Tools

- **Vision:** Layered hierarchy with simple interfaces



Svore et al, IEEE Computer, January 2006

Predictive QC Design Tool

- **Predict performance *before* building!!**

INPUT

-Technology
- Gate performance
- Comm. constraints
- Control capability
- Memory fidelities
- Geometric constraints

- Q. Code
- Entanglement supply

FT Eng. Design Analysis

simulate basic QEC blocks & I/O

OUTPUT

- p_{th} for gates, wires, memory, state supply
- Logical gate speed
- Space, time required

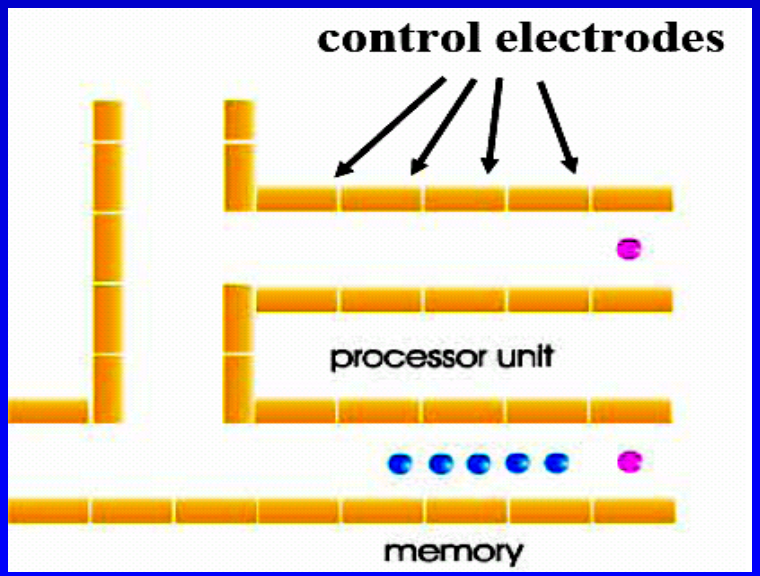
IEEE Computer, 2002 & 2006

a-la cadance, synopsis....

QARC
Quantum Architecture Research Center

Trapped Ion FTQC

- **Wealth of expt. data**
  - Teleportation (3 ions)
  - Superdense coding (2 ions)
  - QFT; Q. error correction (3 ions)
  - GHZ and W states (4-8 ions)
- **Conceptual design**



Kielpinski, Monroe, and Wineland, "Architecture for a Large-Scale Ion-Trap Quantum Computer," Nature 417, 709 (2002)

Timescales	
Single Qubit Gate	1 μs
Two Qubit Gate	10 μs
Measure	100 μs
Cool a linear chain	10 ms
Movement	10 ns / μm
Split a linear chain	1 ms
Join two linear chains	0 seconds
Memory time (not implemented)	100 seconds
Failure Probabilities	
Single Qubit Gate Failure	0.0001
Two Qubit Gate Failure	0.03
Measurement Failure	0.01
Movement Failure	0.005 / μm
Heating <n>	
Moving a Linear Chain	0.01 quanta / μm
Splitting a Linear Chain	1 quanta

If $p_{err}^{meas} \sim 10^{-4} \Rightarrow p_{th} \sim 4 \times 10^{-4}$

Cross (2006)

Trapped ion Factoring?

- Case Study: Quantum Logic Array
  - Trapped ions ; fault tolerant ; NIST parameters

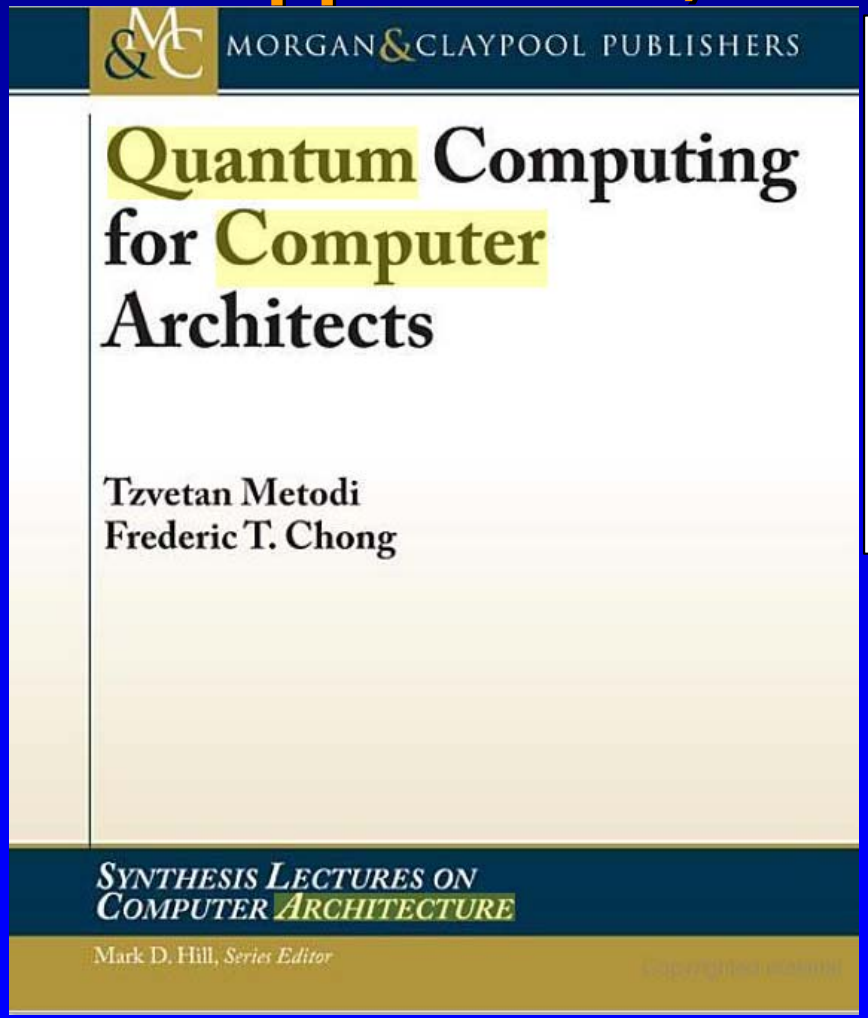


TABLE 9.2: System Numbers for Shor's Algorithm for Factoring an N-bit Number Using the Circuit Descriptions of [154, 155] and the QLA Microarchitecture Model. The QLA Chip Area is Determined by the Number of Logical Qubits and Channels.

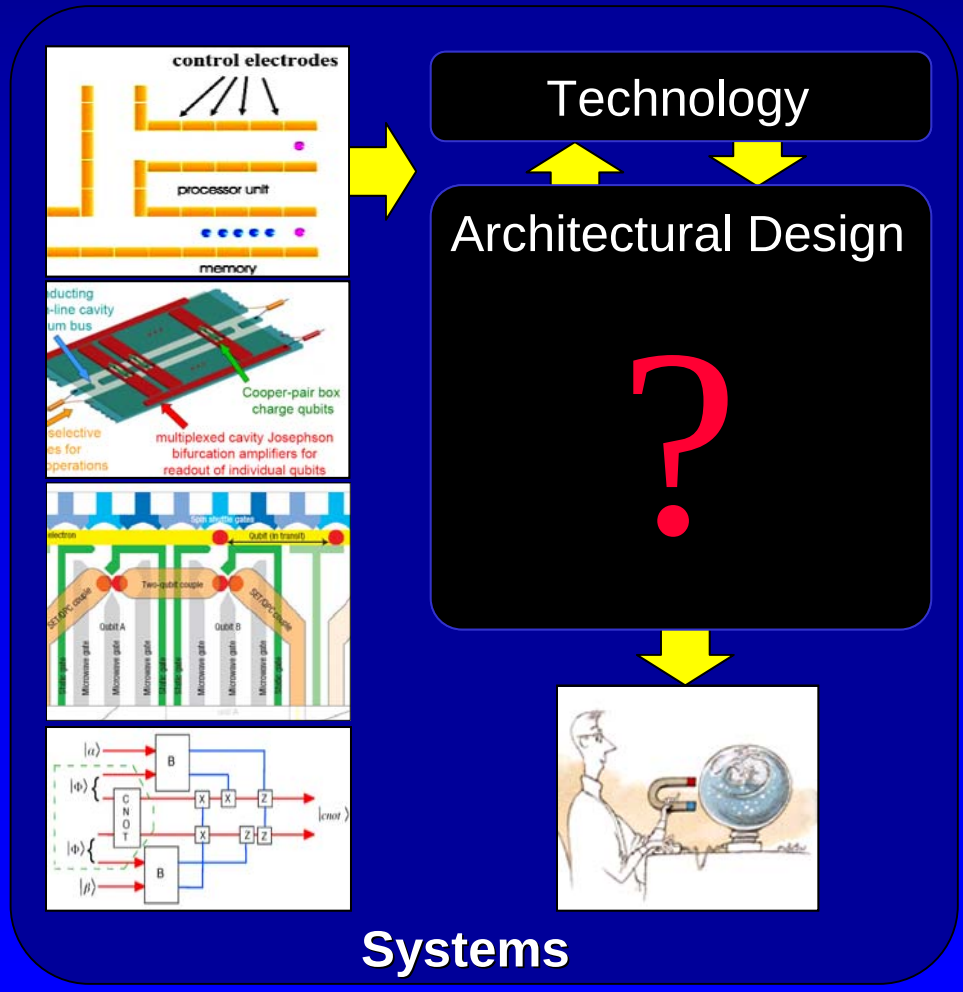
	$N = 128$	$N = 512$	$N = 1024$	$N = 2048$
Logical qubits	37,971	150,771	301,251	602,259
Toffoli gates	63,729	397,910	964,919	2,301,767
Total gates	115,033	1,016,295	3,270,582	11,148,214
Area (m^2)	0.11	0.45	0.90	1.80
Time (days)	0.9	5.5	13.4	32.1

Metodi et al, ISCA 2006

Summary

We are on the verge of being able to build large-scale quantum information processing systems!

- **Architecture is key***
- **Challenges:**
  - **Build predictive tools to DESIGN & VERIFY**
  - **Feedback to strategically improve QC technology**
  - **Contribute back to classical computation (fault tolerance, low power)**



* Science – not just for mission agencies